# 20EC2107 - DIGITAL LOGIC DESIGN

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| Course Category: |  Program Core | Credits: | 3 |
| Course Type: | Theory | Lecture-Tutorial-Practical: | 3-0-0 |
| Prerequisite: | Basic Knowledge on number systems and Boolean Algebra | Sessional Evaluation:Univ. Exam Evaluation:Total Marks: | 4060100 |
| Objectives: | * To understand basic number systems, codes and logical gates.
* To understand the concepts of Boolean algebra.
* To understand the use of minimization logic to solve the Boolean logic expressions.
* To understand the design of combinational circuits.
* To understand the state reduction methods for Sequential circuits.
* To understand the different types of registers and counters.
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| Course Outcomes | Upon successful completion of the course, the students will be able to: |
| CO1 | Identify and explain fundamental concepts of digital logic design including basic and universal gates, number systems, binary coded systems,  |
| CO2 | Learn the Boolean algebra and canonical forms.  |
| CO3 | Review the minimization and simplifications of expressions. |
| CO4 | Study the basic components of combinational and sequential circuits. |
| CO5 | Identify basic components of synchronous sequential circuits  |
| CO6 | Understand the working procedure of counters and registers  |
| Course Content | UNIT-I **Digital Systems and Binary NUMBERS:**Digital Systems, Binary Numbers, Octal and Hexadecimal Numbers, Complements of Numbers, Signed Binary Numbers, Arithmetic addition and subtraction, 4-bit codes: BCD, EXCESS 3, alphanumeric codes, 9’s complement, 2421, etc..UNIT-II **Concept of Boolean ALGEBRA:**Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Canonical And Standard Forms, Conversion Of Canonical Pos To Canonical Sop And Vise Versa.UNIT-III **Gate level MINIMIZATION**:Map, Four Variable K-Maps. Products of Sum Simplification, Sum of Products Simplification, Don’t – Care Conditions, Tabular method, NAND and NOR Implementation, Exclusive OR Function, AOI to NAND logic and AOI to NOR logic implementation.UNIT-IV **Combinational LOGIC:**Introduction, Analysis Procedure, Binary Adder–Subtractor, Binary Multiplier, Decoders, Encoders, Multiplexers, Demultiplexers, Priority Encoder, Code Converters, Magnitude Comparator.UNIT-V **Synchronous Sequential LOGIC:**Introduction to Sequential Circuits, Storage Elements: Latches, Flip-Flops, RS- Latch Using NAND and NOR Gates, Truth Tables. RS, JK, T and D Flip Flops, Truth and Excitation Tables, Conversion of Flip Flops.UNIT-VI **Registers and COUNTERS:**Registers, Shift Registers, Ripple Counters, Synchronous Counters, Ring Counter, Johnson Counter. |
| Text Books &ReferencesBooks | **TEXT BOOKS:**1. Digital Design with an introduction to the Verilog HDL,VHDL and systeamverilog 6th edition by M.Morris Mano Michael D.Ciletti

**REFERENCE BOOKS:**1. Fundamentals of Digital Circuits fourth edition A.Ananda Kumar,
2. A VHDL Primer 3rd edition by J Bhaskar
3. Very log HDL a guide to Digital Design and Synthesis by Samir Palnitkar
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| E-Resources | 1. <https://nptel.ac.in/courses>
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